NEC

MOS FIELD EFFECT TRANSISTOR
2SK2357/2SK2358

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK2357/2SK2358 is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-Resistance
  2SK2357: $R_{DS(on)}$ = 0.9 Ω (V_{GS} = 10 V, I_D = 3.0 A)
  2SK2358: $R_{DS(on)}$ = 1.0 Ω (V_{GS} = 10 V, I_D = 3.0 A)
- Low C_{iss} C_{iss} = 1050 pF TYP.
- High Avalanche Capability Ratings
- Isolate TO-220 Package

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS (T$_A$ = 25 °C)

Drain to Source Voltage (2SK2357/2358)	V_{DSS}	450/500	V
Gate to Source Voltage	V_{GSS}	±30	V
Drain Current (DC)	$I_{D(DC)}$	±6.0	A
Drain Current (pulse)*	$I_{D(pulse)}$	±24	A
Total Power Dissipation (T$_c$ = 25 °C)	P_{T1}	35	W
Total Power Dissipation (T$_a$ = 25 °C)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Single Avalanche Current**	I_{AS}	6.0	A
Single Avalanche Energy**	E_{AS}	17	mJ

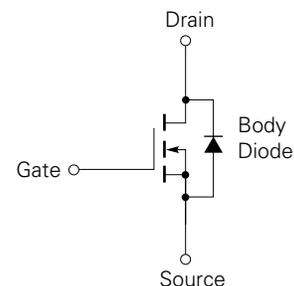* PW $\leq$ 10 μs, Duty Cycle $\leq$ 1 %
** Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V $\rightarrow$ 0

PACKAGE DIMENSIONS
(in millimeters)
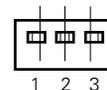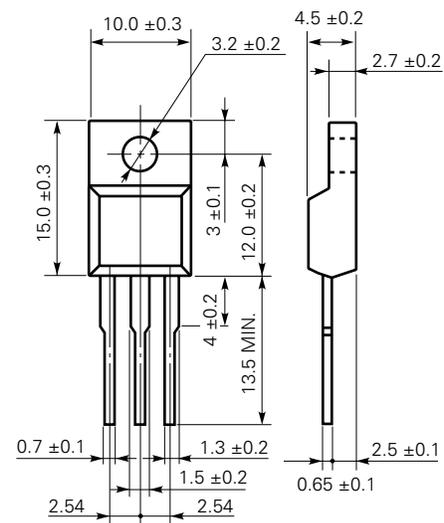

1. Gate
2. Drain
3. Source

MP-45F (ISOLATED TO-220)

ELECTRICAL CHARACTERISTICS (T$_A$ = 25 °C)

| CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Drain to Source On-Resistance	R$_{DS(on)}$		0.7	0.9	Ω	V$_{GS}$ = 10 V	2SK2357
			0.8	1.0		I$_D$ = 3.0 A	2SK2358
Gate to Source Cutoff Voltage	V$_{GS(off)}$	2.5		3.5	V	V$_{DS}$ = 10 V, I$_D$ = 1 mA	
Forward Transfer Admittance	| y$_{fs}$ |	3.0			S	V$_{DS}$ = 10 V, I$_D$ = 3.0 A	
Drain Leakage Current	I$_{DSS}$			100	μA	V$_{DS}$ = V$_{DSS}$, V$_{GS}$ = 0	
Gate to Source Leakage Current	I$_{GSS}$			±100	nA	V$_{GS}$ = ±30 V, V$_{DS}$ = 0	
Input Capacitance	C$_{iss}$		1050		pF	V$_{DS}$ = 10 V	
Output Capacitance	C$_{oss}$		200		pF	V$_{GS}$ = 0	
Reverse Transfer Capacitance	C$_{rss}$		26		pF	f = 1 MHz	
Turn-On Delay Time	t$_{d(on)}$		14		ns	I$_D$ = 3.0 A	
Rise Time	t$_r$		9		ns	V$_{GS(on)}$ = 10 V	
Turn-Off Delay Time	t$_{d(off)}$		56		ns	V$_{DD}$ = 150 V	
Fall Time	t$_f$		14		ns	R$_G$ = 10 Ω R$_L$ = 50 Ω	
Total Gate Charge	Q$_G$		27		nC	I$_D$ = 6.0 A	
Gate to Source Charge	Q$_{GS}$		5.5		nC	V$_{DD}$ = 400 V	
Gate to Drain Charge	Q$_{GD}$		12		nC	V$_{GS}$ = 10 V	
Body Diode Forward Voltage	V$_{F(S-D)}$		1.0		V	I$_F$ = 6.0 A, V$_{GS}$ = 0	
Reverse Recovery Time	t$_{rr}$		300		ns	I$_F$ = 6.0 A, V$_{GS}$ = 0	
Reverse Recovery Charge	Q$_{rr}$		1.5		nC	di/dt = 50 A/μs	

Test Circuit 1 Avalanche Capability
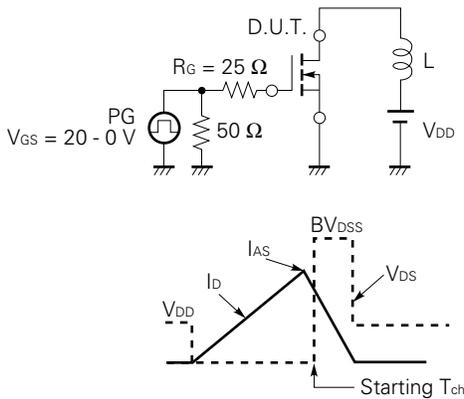
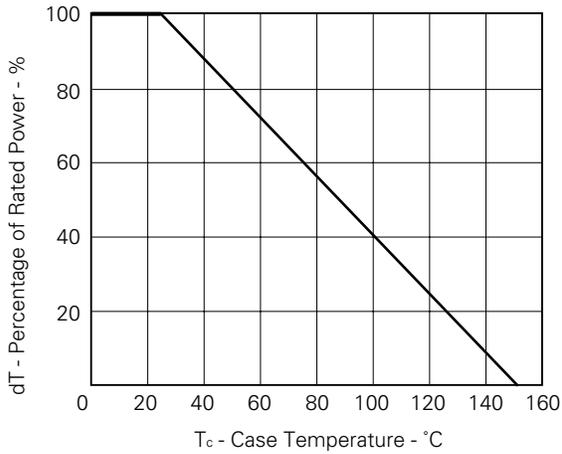**Test Circuit 2 Switching Time**
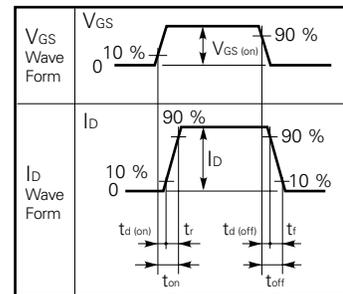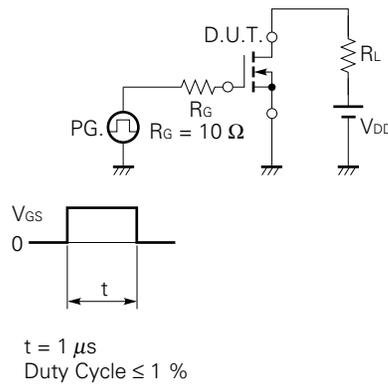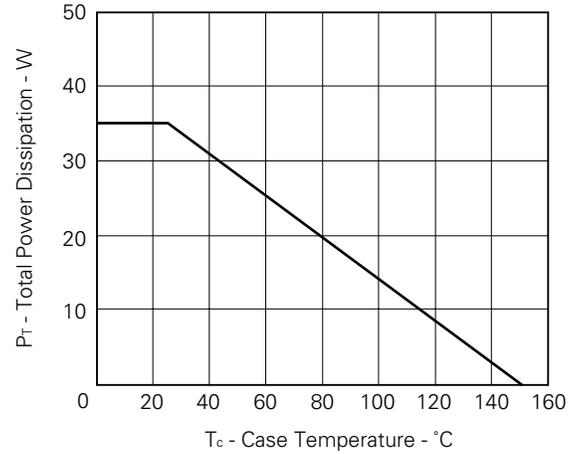

Test Circuit 3 Gate Charge
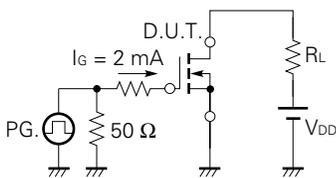
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.
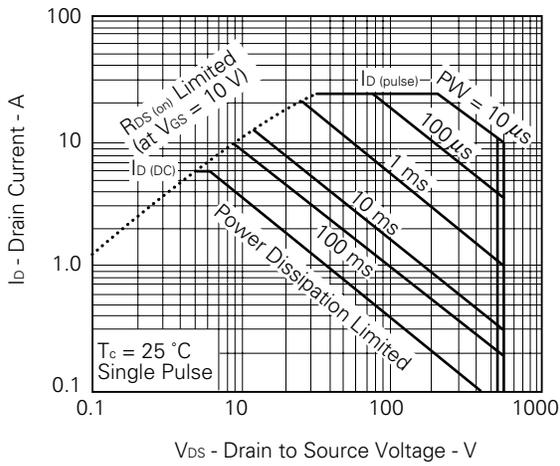
TYPICAL CHARACTERISTICS (T$_A$ = 25 ˚C)

DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREA

dT - Percentage of Rated Power - %

T$_c$ - Case Temperature - ˚C

TOTAL POWER DISSIPATION vs.
CASE TEMPERATURE

P$_T$ - Total Power Dissipation - W

T$_c$ - Case Temperature - ˚C

FORWARD BIAS SAFE OPERATING AREA

I$_D$ - Drain Current - A

R$_{DS (on)}$ Limited
(at V$_{GS}$ = 10 V)

I$_D$ (pulse)

PW = 10 µs

100 µs

1 ms

10 ms

100 ms

I$_D$ (DC)

Power Dissipation Limited

T$_c$ = 25 ˚C
Single Pulse

V$_{DS}$ - Drain to Source Voltage - V

DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

I$_D$ - Drain Current - A

Pulsed

V$_{GS}$ = 20 V
10 V
8 V
6 V

V$_{DS}$ - Drain to Source Voltage - V
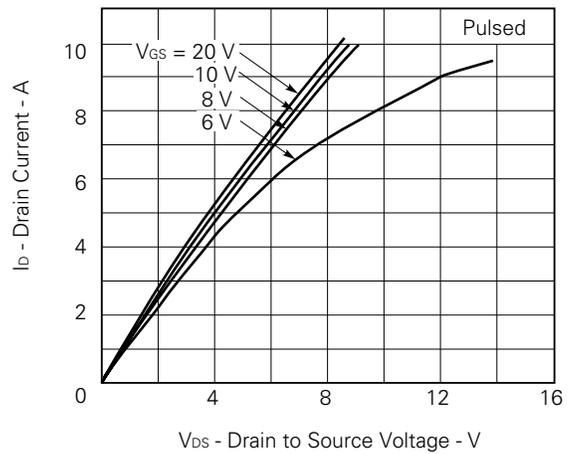
DRAIN CURRENT vs.
GATE TO SOURCE VOLTAGE

I$_D$ - Drain Current - A

Pulsed

T$_a$ = −25 ˚C
25 ˚C
75 ˚C
125 ˚C

V$_{GS}$ - Gate to Source Voltage - V

3
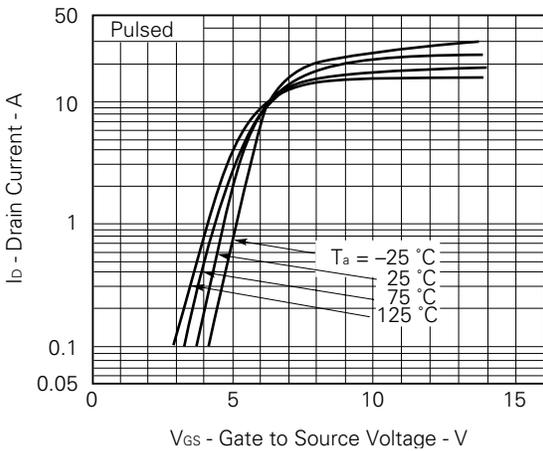
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

Plot: $r_{th(ch-c)}(t)$ - Transient Thermal Resistance - °C/W vs. PW - Pulse Width - s. Curves labeled $R_{th(ch-a)} = 62.5$ °C/W and $R_{th(ch-c)} = 3.57$ °C/W. $T_C = 25$ °C, Single Pulse.
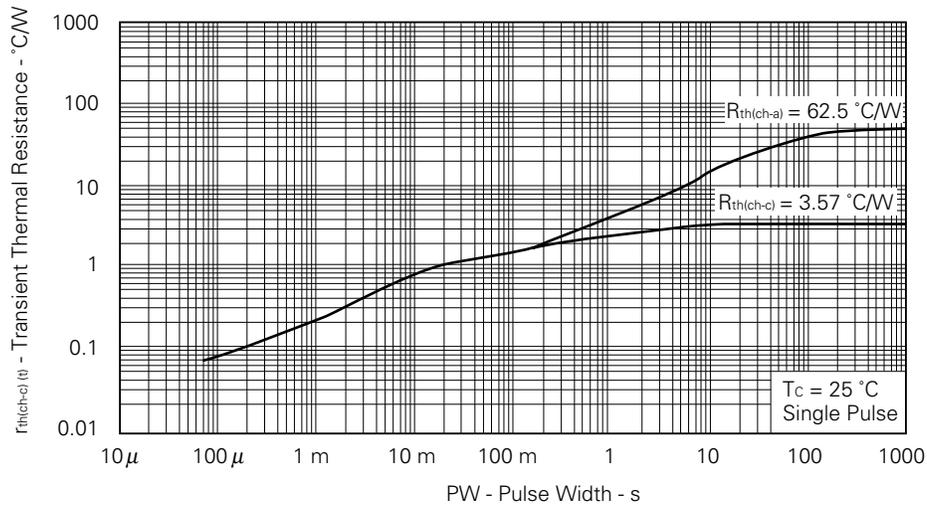
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

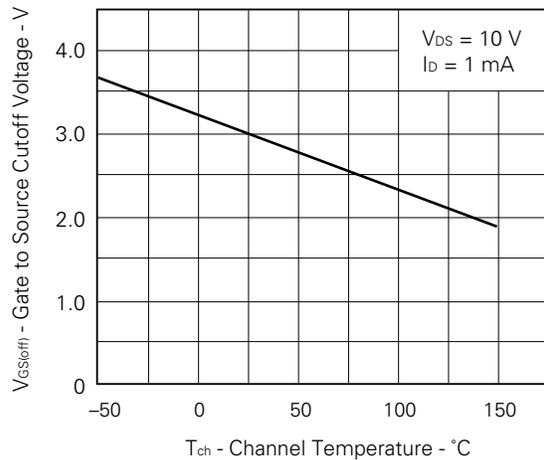Plot: |yfs| - Forward Transfer Admittance - S vs. I_D - Drain Current - A. $V_{DS} = 10$ V, Pulsed. $Ta = -25$ °C, 25 °C, 75 °C, 125 °C.
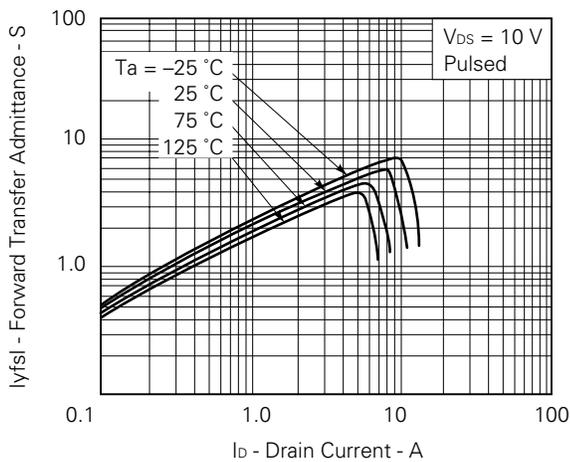
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

Plot: $R_{DS(on)}$ - Drain to Source On-State Resistance - Ω vs. V_{GS} - Gate to Source Voltage - V. Pulsed. $I_D = 6$ A, $I_D = 3$ A.
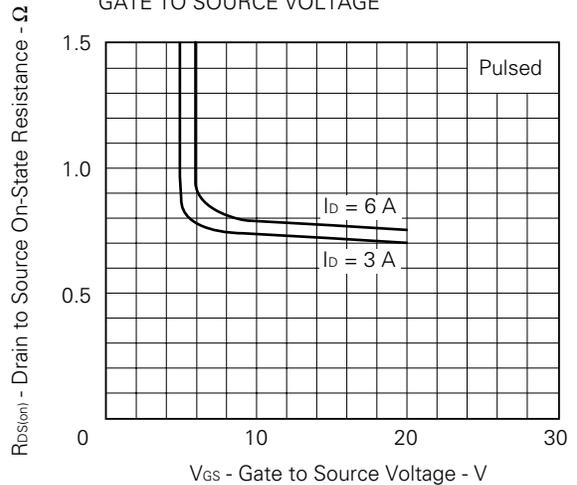
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

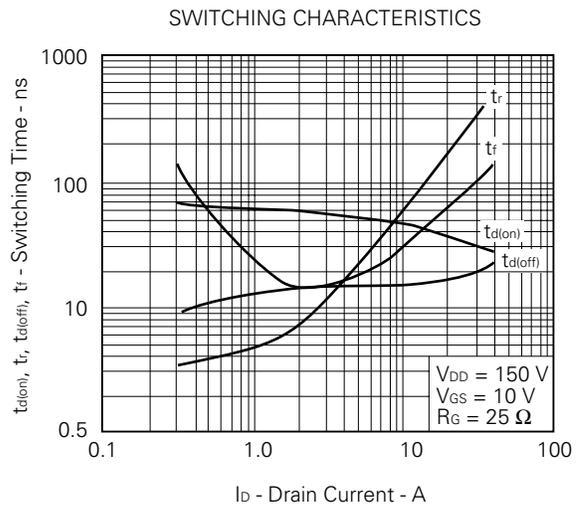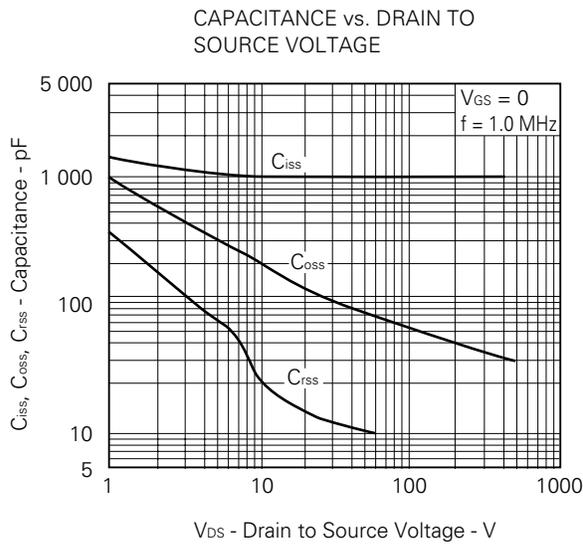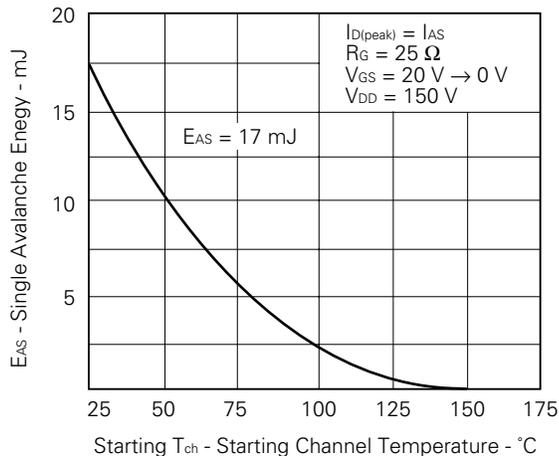Plot: $R_{DS(on)}$ - Drain to Source On-State Resistance - Ω vs. I_D - Drain Current - A. Pulsed.
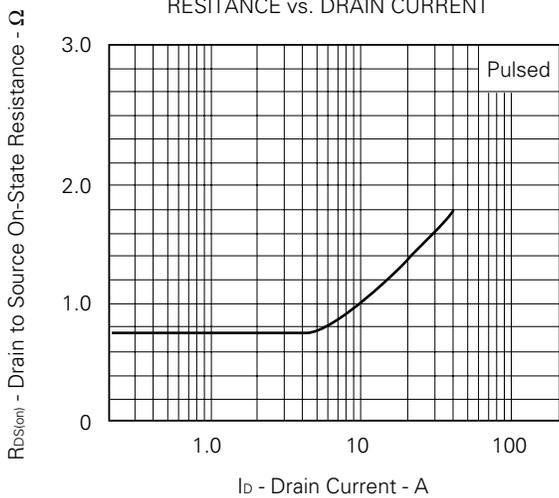
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

Plot: $V_{GS(off)}$ - Gate to Source Cutoff Voltage - V vs. T_{ch} - Channel Temperature - °C. $V_{DS} = 10$ V, $I_D = 1$ mA.

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE

$R_{DS(on)}$ - Drain to Source On-State Resistance - Ω

I_D = 6 A
3 A

V_{GS} = 10 V

T_{ch} - Channel Temperature - °C

SOURCE TO DRAIN DIODE
FORWARD VOLTAGE

I_{SD} - Diode Forward Current - A

Pulsed

10 V V_{GS} = 0

V_{SD} - Source to Drain Voltage - V

CAPACITANCE vs. DRAIN TO
SOURCE VOLTAGE

C_{iss}, C_{oss}, C_{rss} - Capacitance - pF

V_{GS} = 0
f = 1.0 MHz

C_{iss}

C_{oss}

C_{rss}

V_{DS} - Drain to Source Voltage - V

SWITCHING CHARACTERISTICS

$t_{d(on)}$, t_r, $t_{d(off)}$, t_f - Switching Time - ns

t_r
t_f
$t_{d(on)}$
$t_{d(off)}$

V_{DD} = 150 V
V_{GS} = 10 V
R_G = 25 Ω

I_D - Drain Current - A

REVERSE RECOVERY TIME vs.
DRAIN CURRENT

t_{rr} - Reverse Recovery Diode - ns

di/dt = 50 A/ μs
V_{GS} = 10 V

I_D - Drain Current - A

DYNAMIC INPUT/OUTPUT CHARACTERISTICS

V_{DS} - Drain to Source Voltage - V

V_{GS} - Gate to Source Voltage - V

I_D = 6 A

V_{DD} = 400 V V_{GS}
250 V
125 V

V_{DS}

Q_g - Gate Charge - nC

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SINGLE AVALANCHE ENERGY vs
STARTING CHANNEL TEMPERATURE

$I_{D(peak)} = I_{AS}$
$R_G = 25\ \Omega$
$V_{GS} = 20\ V \rightarrow 0\ V$
$V_{DD} = 150\ V$

$E_{AS} = 17\ mJ$

E_{AS} - Single Avalanche Enegy - mJ

Starting T_{ch} - Starting Channel Temperature - ˚C

SINGLE AVALANCHE CURRENT vs
INDUCTIVE LOAD

$R_G = 25\ \Omega$
$V_{DD} = 150\ V$
$V_{GS} = 20\ V \rightarrow 0$
Starting $T_{ch} = 25$˚C

$I_{AS} = 6.0\ A$

$E_{AS} = 17\ mJ$

I_{AS} - Single Avalanche Current - A

L - Inductive Load - H
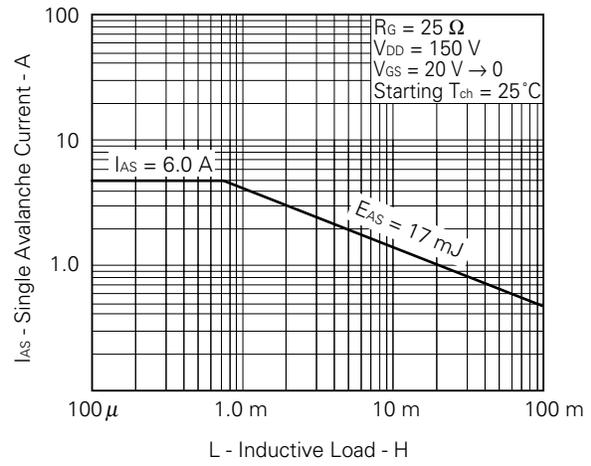
REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

    The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

M4 92.6